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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/791,249	FISKE, MICHAEL	
	Examiner	Art Unit	
	Benjamin Buss	2129	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 April 2007 and 23 July 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,5,6,8-18,21,23-29,31,32 and 34-62* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5,6,8-18,21,23-29,31,32 and 34-62* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *7/23/2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/19/2007*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to an AMENDMENT entered 7/23/2007 for the patent application 10/791,249 filed on 3/2/2004, which claims priority based on 60/456,715 filed on **3/24/2003**. The Office Action of 12/14/2006 is fully incorporated into this Office Action by reference. Claims 1, 2, 5, 6, 8-18, 21, 23-29, 31, 32, and 34-62 are pending in this application.

Specification

Response to Arguments

Applicant's arguments, see page 22, filed 7/23/2007, with respect to the objections to the specification have been fully considered and are persuasive. The objections to the specification have been withdrawn.

Drawings

Response to Arguments

Applicant's arguments, see pages 22-23, filed 7/23/2007, with respect to the objections to the drawings have been fully considered and are persuasive. The objections to the specification have been withdrawn.

Claim Objections

Claims 1, 5, 8, 11, 13-14, 16-17, 26-27, 63-38, 40, 48-49, and 52-55 are objected to because of the following informalities:

- Claims 5, 8, and 14 objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. These claims do not further limit the machine of claim 1. Examiner suggests the claims be rewritten in independent form to clearly delineate the required limitations.
- Claim 1 (Line 7): Change "Effectors behave and" to -- Effectors behave, and --.
- Claim 8 (Line 2): Change "machine of claim 1. and ..." to -- machine of claim 1; and --.
- Claim 11 (Lines 3, 5, & 6): Change "meta program" to -- Meta program --.
- Claim 13: Change "gate voltage at which the mobile charge in the transistor begins to limit the flow of current is called the threshold voltage" to -- gate voltage, called the threshold voltage, at which the mobile charge in the transistor begins to limit the flow of current --.

- Claim 14 (Line 3): Change "effector machine" to -- Effector machine --.
- Claim 16 (Lines 4, 5, 6, 8, 9, & 10): Change "effectors" to -- Effectors --.
- Claim 17 (Line 8): Change "Effectors behave and" to -- Effectors behave, and --.
- Claim 26 (Line 2): Change "effectors" to -- Effectors --.
- Claim 27 (Line 6): Change "meta program" to -- Meta program --.
- Claim 36 (Lines 3-4): Change "computing elements. the Effector machine is a first Effector machine and" to -- computing elements, the Effector machine is a first Effector machine, --.
- Claim 36 (Line 9): Change "of hardware computing elements" to -- of hardware computing elements. --.
- Claim 37 (Line 2): Change "meta program" to -- Meta program --.
- Claim 38 (Lines 1 & 2): Change "effector machine" to -- Effector machine --.
- Claim 38 (Line 9): Change "meta program" to -- Meta program --.
- Claim 40 (Line 2): Change "effectors" to -- Effectors --.
- Claim 48 (Line 3): Change "meta program" to -- Meta program --.
- Claim 49 (Lines 3, 4, & 5): Change "meta program" to -- Meta program --.
- Claim 52 (Lines 3-4): Change "Meta program. the meta program" to -- Meta program, the Meta program --.
- Claim 53 (Lines 7-8): Change "meta program" to -- Meta program --.
- Claim 54 (Line 3): Change "meta program" to -- Meta program --.
- Claim 55 (Line 3): Change "meta program" to -- Meta program --.

Appropriate correction is required.

Claim Rejections - 35 USC § 101

Response to Arguments

Applicant's arguments, see pages 23-27, filed 7/23/2007, with respect to the rejections under 35 U.S.C. §101 have been fully considered and are persuasive. The rejections of claims 1, 2, 5, 6, 8-18, 21, 23-29, 31, 32, and 34-58 have been withdrawn.

Claim Rejections - 35 USC § 112

Response to Arguments

Applicant's arguments, see pages 26-31, filed 7/23/2007, with respect to the rejections under 35 U.S.C. §112, first paragraph, have been fully considered and are persuasive. The rejections of claims 1, 2, 5, 6, 8-18, 21, 23-29, 31, 32, and 34-58 have been withdrawn.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-2, 5-6, 8-18, 21, 23-29, 31-32, and 34-62 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

- Claim 1 recites: " ... adjusts how the Effectors behave ... adjusts how information is transmitted ..."
  - Examiner does not understand what this limitation means or is intended to cover. It is not clear what behaviors the Effectors can be adjusted between. It is not clear from what set of transmission methods the Effector information transmittal is chosen.
- Claim 5 recites: "A system comprising an input interpreter ... for designing at least the machine of claim 1..."
  - **It is unclear if it is necessary to actually possess the invention of claim 1 in order to have the system of claim 5.** The claim dependency is declared within an "intended use" clause, thereby putting "the machine of claim 1" into a portion of the claim which does not affect the patentability of the claim, making the dependence unclear. **Examiner suggests that this claim be written in independent form to clearly delineate the required limitations.**
- Claim 12 recites: "...said machine architecture comprises hardware having a predetermined error tolerance..."
  - It is unclear what kind of "error" the tolerance limits.
- The term "at least partially" in claims 14, 47, and 48 is a relative term that renders the claim indefinite. The term "at least partially" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. It is not clear to what extent the claim requires the task to be performed. "At least

partially" could be interpreted to mean any trivially miniscule portion of the recited task, such as opening a file, changing a single value, or saving a file in an appropriate output.

- Claim 16 recites the limitation "software machine" in line 3. There is insufficient antecedent basis for this limitation in the claim.
- Claim 17 recites: " ... adjusts how Effectors behave ... adjusts how information is transmitted ..."
    - Examiner does not understand what this limitation means or is intended to cover. It is not clear what behaviors the Effectors can be adjusted between. It is not clear from what set of transmission methods the Effector information transmittal is chosen.
- Claim 28 recites: "... based on an error tolerance."
    - It is unclear what kind of "error" the tolerance limits.
- Claim 32 recites the limitation "software machine" in line 3. There is insufficient antecedent basis for this limitation in the claim.
- Claim 40 recites the limitation "software module" in line 2. There is insufficient antecedent basis for this limitation in the claim.
- Claim 41 recites the limitation "software Effectors" in line 3. There is insufficient antecedent basis for this limitation in the claim.
- Claim 42 recites the limitation "software Effectors" in lines 2-3. There is insufficient antecedent basis for this limitation in the claim.
- Claim 43 recites the limitation "software Effectors" in line 3. There is insufficient antecedent basis for this limitation in the claim.
- Claim 47 recites "... at least partially designing at least a Static program ..."
    - It is unclear what it means for the system of claim 47 to be "at least partially designing at least a Static program for the Effector machine": It is not clear what constitutes "partially designing" such a program. Any computer should meet the limitations of this claim.
- Claim 48 recites "... at least partially designing at least a Meta program ..."
    - It is unclear what it means for the system of claim 48 to be "at least partially designing at least a Meta program for the Effector machine". It is not clear what constitutes "partially designing" such a program. Any computer should meet the limitations of this claim.

- Claim 60 recites: " ... determines how the software Effectors behave ... determines how information is transmitted ..."
    - Examiner does not understand what this limitation means or is intended to cover. It is not clear what behaviors the Effectors can be adjusted between. It is not clear from what set of transmission methods the Effector information transmittal is chosen.
- Claim 61 recites: " ... determines how Effectors behave ... determines how information is transmitted ..."
    - Examiner does not understand what this limitation means or is intended to cover. It is not clear what behaviors the Effectors can be adjusted between. It is not clear from what set of transmission methods the Effector information transmittal is chosen.
- Claim 62 recites: " ... determines how the Effectors behave ... determines how information is transmitted ..."
    - Examiner does not understand what this limitation means or is intended to cover. It is not clear what behaviors the Effectors can be adjusted between. It is not clear from what set of transmission methods the Effector information transmittal is chosen.
- Claims 2, 5-6, 8-16, 18, 21, 23-29, 31-32, and 34-59 are rejected due to their dependence on rejected claims since they do not overcome the outstanding rejections.

Appropriate corrections are required.

Response to Arguments

Applicant's arguments, see pages 31-37, filed 7/23/2007, with respect to the rejection of claims 6, 8, 11, 13, 18, 26-27,36, 38, and 49-58 have been fully considered and are persuasive. However, these claims are still rejected by virtue of their dependence on a rejected base claim.

Applicant's arguments filed 7/23/2007 have been fully considered but they are not persuasive. In re pages 31-32, Applicant argues that claims 8, 14, 47, and 48 are proper claim constructions. Examiner agrees that the amended claims do not merit §112 rejections for the construction.

In re pages 33-34, Applicant argues that that "the word partially has been deleted from claims 5, 14, 47, and 48, thereby obviating this ground of rejection. Examiner agrees for claim 5 only. Examiner disagrees for claims 14, 47, and 48. The word partially has not been deleted. The phrase "at least partially" is still not defined in the claim and the specification still does not provide a standard for ascertaining the requisite degree. Claims 14, 47, and 48 remain rejected on this basis.

In re pages 33-34, Applicant argues that there is no need for claims 5, 47, and 48 to recite "how", since this makes the claim generic and broad, not indefinite. Examiner disagree insofar as it is still not clear what it means for the systems of claims 47 and 48 to "at least partially" design a program. What are the intended metes and bounds of these claims?

Claim Rejections - 35 USC § 102

Response to Arguments

Applicant's arguments with respect to claims 1, 5, 17, 47, and 48 have been considered but are moot in view of the new ground(s) of rejection.

In re page 37, Applicant argues that "the terms 'Effector' and 'Effector machine' that appear in the claims are defined by the claim and are **not defined by the definition in the specification**" (emphasis added). Applicant has admitted that the claims use different definitions than the specification. Is the same "Effector" discussed in the claim and specification? Is the current definition claimed fully supported by the original disclosure as filed?

Based on the claim limitations these terms refer to, the Examiner has reasonably mapped all limitations to neural network art, as detailed below.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-2, 5-6, 8, 10-12, 14-18, 21, 23-24, 26-28, 31-32, 34-35, 37-38, 43, 45, and 47-62 are rejected under 35 U.S.C. 102(b) as being anticipated by **de Garis** ("The CAM-Brain Machine (CBM): an FPGA-based hardware tool that evolves a 1000 neuron-net circuit module in seconds and updates a 75 million neuron artificial brain for real-time robot control").

Claims 1 and 17:

de Garis anticipates:

- providing a hardware computing machine, which will be called an Effector machine by at least (p35-67 especially "artificial brain" §5.1; *Calling the computing machine an "Effector machine" is simply labeling it and constitutes merely non-functional descriptive material which does not affect patentability – any "hardware computing machine" is reasonably interpreted to meet the claimed "Effector machine" in this Application*):
    - (a) providing a collection of hardware computing elements, which will be referred to as Effectors (p35-67 especially "neurons" §5.1; *Calling the computing elements "Effectors" is simply labeling them and constitutes merely non-functional descriptive material which does not affect patentability – any "hardware computing element" is reasonably interpreted to meet the claimed "Effectors" in this Application*);
    - (b) communicatively coupling each Effector of the collection to at least one other Effector (p35-67 especially "neurons are densely interconnected" §5.1 or "external connections to provide signal input from other modules" §5.2.1);
    - (c) providing a machine architecture that, while the machine is running, adjusts how the computing elements behave and adjusts how information is transmitted from one computing element to another computing element (C35-67 especially "interconnected with branching dendritic and axonic trees ... forming hundreds of connections ... evolved directly in hardware ... population of chromosomes, which represent neural networks of different topologies and functionalities" §5.1 or §5.2.2).

Claims 2:

de Garis anticipates:

- wherein a subset of said Effectors are configured to receive information from a Static program (p35-67 especially "spiketrains (bit strings of 0s and 1s) to be input" §1 or "input is converted automatically to a spiketrain, which enters the neural net module" §3.1 or "instantiated" §5.2.1 or "preprogrammed" §5.3 or "would not modify themselves based on their runtime experience" §8.2 or "an initiating input arrives" §8.2; *A "subset of said Effectors" is interpreted to be any set containing <u>at least one</u> of said Effectors. This interpretation includes the subset of the whole, in which <u>all</u> of said Effectors are part of the subset*).

Claim 5:

de Garis anticipates:

- a computer readable medium storing thereon one ore more instructions that constitute an input interpreter, the input interpreter outputs a software Effector machine which is a design for the hardware Effector machine (p35-67 especially "CBM" §5.1 or "module interconnection netlist" §5.2.5; *The phrase "for designing at least the machine of claim 1" is interpreted to be an intended use, and therefore does not further limit the claim*).

Claim 6:

de Garis anticipates:

- wherein the software Effector machine is a first software Effector machine, said input interpreter is implemented with a second Effector machine that includes at least a second collection of software computing elements (p35-67 especially "CBM" §5.1 or "software" §6; *The person of ordinary skill in the art at the time the invention was made would have logically understood that the CBM software could be the second Effector machine which implements the input interpreter*).

Claim 8:

de Garis anticipates:

- the Effector machine of claim 1 (p35-67 as detailed above), and
- an output interpreter in addition to the Effector machine (p35-67 especially "interpretation in order to interpret the spiketrain output" §4 or "modules" §5.1; *The phrase "wherein the interpreter is for translating firing activity of a subset of Effectors into a desired output form" is interpreted to be an intended use, and therefore does not further limit the claim*).

Claims 10 and 26:

de Garis anticipates:

- wherein said machine is a dynamic machine in that one or more parameters of the Effectors are functions of time (p36-67 especially ""time-dependent signals" §1 or "time-dependent signal" §3.1 or "time-shifted spiketrain" §3.2).

Claims 11 and 27:

de Garis anticipates:

- the machine (p36-67 as detailed above; *The claim is interpreted to be directed to an intended use, and therefore does not further limit the parent claim*).

Claims 12 and 28:

de Garis anticipates:

- wherein said machine architecture comprises hardware having a predetermined error tolerance by limiting a range of values to which one or more parameters of the hardware are allowed to be set (p35-67 especially "preprogrammed to shut off the main clock when a temperature limit is exceeded" §5.3).

Claims 14 and 23:

de Garis anticipates:

- designing the machine of claim 1, at least partially, by evolving a graph representing the machine to produce a design of the Effector machine (p36-67 especially §5.1 or §7.3).

Claims 15 and 31:

de Garis anticipates:

- wherein the evolving of the graph includes at least performing a crossover of two representations of Effector machines via interchanging representations of modules of the two representations of Effector machines (p36-67 especially §5.2 or §5.2.4).

Claim 16:

de Garis anticipates:

- wherein the evolving of the graph (p36-67 as detailed above for claim 14; *The claim is interpreted to be directed to an intended use, and therefore does not further limit the parent claim*).

Claims 18, 51, and 52:

de Garis anticipates:

- wherein a subset of said Effectors exists (p36-67 especially §5.1; *Calling the subset "Input Effectors" is simply labeling it and constitutes merely non-functional descriptive material which does not affect patentability; The remainder of the claim is interpreted to be an intended use, and therefore does not further limit the claim*).

Claim 21:

de Garis anticipates:

- designing the Effector machine via an input interpreter (p35-67 especially "CBM" §5.1 or "module interconnection netlist" §5.2.5).

Claim 24:

de Garis anticipates:

- configuring a subset of said Effectors (p36-67 especially §5.1 or §5.2; *Calling the subset "Output Effectors" is simply labeling it and constitutes merely non-functional descriptive material which does not affect patentability; The phrase "for translating at least one firing activity of the Output Effectors into a desired output form" is interpreted to be an intended use, and therefore does not further limit the claim*).

Claim 32:

de Garis anticipates:

- wherein evolving the graph includes at least changing one or more of the following properties associated with at least a portion of a representation of the machine:
    - a number of software modules per software machine,

- a number of software effectors per software modules,
- a refractory period associated with at least one of the software Effectors,
- a threshold associated with a software Effector,
- a number of software connections between the software Effectors (p36-67 especially §5.1),
- an amplitude associated with one or more of the software Effectors,
- a pulse width associated with one or more of the software Effectors (p36-67 especially §6), and
- a conduction time between at least two of the software Effectors.

Claim 34:

de Garis anticipates:

- designing at lest one circuit that is associated with the machine by at least evolving a graph associated with the circuit (p36-67 especially §5.1 or §7.3).

Claim 35:

de Garis anticipates:

- wherein a subset of said Effectors are configured to receive information from an external environment (p36-67 especially §2 or §5.2 or §5.2.3 or §5.2.6; *The phrase "configured to receive information from an external environment" is interpreted to be merely a design choice*).

Claim 37:

de Garis anticipates:

- wherein a subset of said Effectors are configured to receive information from a Meta program, the Meta program being a sequence of sets, each set being a list of values of parameters of Effectors (p36-67 especially §2 or §3.1 or §5.2 or §5.2.3 or §5.2.6 or §8.2; *The phrase "configured to receive information from a Meta program ..." is interpreted to be merely a design choice*).

Claim 38:

de Garis anticipates:

- wherein the Effector machine is a first Effector machine, a subset of said Effectors (p35-67 as detailed above; *The remainder of the claim is interpreted to be an intended use, and therefore does not further limit the claim*).

Claim 43:

de Garis anticipates:

- wherein said evolving of the graph includes at least changing a number of software connections between two or more software Effectors (p36-67 especially §5.1).

Claim 45:

de Garis anticipates:

- wherein said evolving of the graph includes at least changing one or more representations of pulse widths associated with representations of the Effectors (p36-67 especially §6).

Claims 47 and 48:

de Garis anticipates:

- further comprising an input interpreter (p35-67 especially "CBM" §5.1 or "module interconnection netlist" §5.2.5; *The remainder of the claim is interpreted to be an intended use, and therefore does not further limit the claim*).

Claim 49:

de Garis anticipates:

- wherein the machine (p35-67 as detailed above; *The remainder of the claim is interpreted to be an intended use, and therefore does not further limit the claim*).

Claims 50 and 53:

de Garis anticipates:

- wherein the Effector machine is a first Effector machine, a subset of said Effectors exists (p36-67 especially §5.1; *Calling the subset "Input Effectors" is simply labeling it and constitutes merely non-functional descriptive material which does not affect patentability; Likewise for calling the Effector machine "a first Effector machine"; The remainder of the claim is interpreted to be an intended use, and therefore does not further limit the claim*).

Claims 54, 55, 56, 57, and 58:

de Garis anticipates:

- wherein the dynamic machine (p36-67 as detailed above; *The claim is interpreted to be directed to an intended use, and therefore does not further limit the parent claim*).

Claim 59:

de Garis anticipates:

- the system (p36-67 as detailed above; *The phrase "being configured such that the interpreter interprets whether an Effector fires as binary information, and interprets the binary information into the desired output form, which includes at least a sequence of symbols" is interpreted to be merely a design choice*).

Claim 60:

de Garis anticipates:

- a machine readable medium storing instructions (p36-67 especially "large RAM memory space" §1 or "module interconnection memory" §2 or "memory" §5.2.2 or §5.2.5; *The remainder of the claim is interpreted to be directed to an intended use, and therefore does not further limit the claim, though the limitations are mapped to the art in rejections found above*).

Claims 61 and 62:

de Garis anticipates:

- a hardware computing machine, which will be called an Effector machine by at least (p35-67 especially "artificial brain" §5.1; *Calling the computing machine an "Effector machine" is simply labeling it and constitutes merely non-functional descriptive material which does not affect patentability – any "hardware computing machine" is reasonably interpreted to meet the claimed "Effector machine" in this Application*):
    - (a) providing a collection of hardware computing elements, which will be referred to as Effectors (p35-67 especially "neurons" §5.1; *Calling the computing elements "Effectors" is simply labeling them and constitutes merely non-functional descriptive material which does not affect patentability – any "hardware computing element" is reasonably interpreted to meet the claimed "Effectors" in this Application*);
    - (b) providing a machine architecture that adjusts how the computing elements behave and adjusts how information is transmitted from one computing element to another computing element (C35-67 especially "interconnected with branching dendritic and axonic trees ... forming hundreds of connections ... evolved directly in hardware ... population of chromosomes, which represent neural networks of different topologies and functionalities" §5.1 or §5.2.2).
    - (c) configuring each Effector of the collection to be communicatively coupled to at least one other Effector (p35-67 especially "neurons are densely interconnected" §5.1 or "external connections to provide signal input from other modules" §5.2.1; *Furthermore, the phrase "configuring each Effector of the collection to be communicatively coupled to at least one other Effector" is interpreted to be merely a design choice which does not affect the patentability of the claim*); and
    - (d) configuring a portion of the hardware computing machine for receiving input that sets values for one or more parameters of individual Effectors from the collections of Effectors, the one or more parameters including a time at which information is transmitted from the individual Effectors to another of the individual Effectors (p35-67 especially "time 't'" §3.2 or "time-dependent" §3.2 or "external connections to provide signal input from other modules" §5.2.1 or "time-shared" §5.2.1 or "propagation time" §5.2.1 or "the same time" §5.2.3 or §7.2 or "time-dependent" §8.1; *Furthermore, the phrase "configuring a portion of the hardware computing machine for receiving input that sets values for one*

or more parameters of individual Effectors from the collections of Effectors, the one or more parameters including a time at which information is transmitted from the individual Effectors to another of the individual Effectors" is interpreted to be merely a design choice which does not affect the patentability of the claim).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 9 and 25 rejected under 35 U.S.C. 103(a) as being unpatentable over **de Garis** ("The CAM-Brain Machine (CBM): an FPGA-based hardware tool that evolves a 1000 neuron-net circuit module in seconds and updates a 75 million neuron artificial brain for real-time robot control") as applied to claims 1-2, 5-6, 8, 10-12, 14-18, 21, 23-24, 26-28, 31-32, 34-35, 37-38, 43, 45, and 47-62 above, and further in view of **Siegelmann** ("Neural Networks and Analog Computation: Beyond the Turing Limit") and **Azam** ("Biologically Inspired Modular Neural Networks").

Claim 9 and 25:

de Garis teaches:

- the collection of hardware computing elements is a first collection of hardware computing elements (p35-67 especially "neurons" §5.1),
- the Effector machine is a first Effector machine (p35-67 especially "artificial brain" §5.1),
- the translating is performed via an output interpreter (p35-67 especially "interpretation in order to interpret the spiketrain output").

de Garis fails to explicitly teach:

- the output interpreter being implemented with a second Effector machine that is constructed from a second collection of hardware computing elements, and
- the first collection of hardware elements and the second collection of hardware elements are different subsets of a third collection of hardware computing elements.

Siegelmann teaches:

- implementing the output interpreter with a second Effector machine that is constructed from a second collection of hardware computing elements (p29-33 and p153-164 especially "it is possible to specify a network that simulates a universal Turing machine in real time" page 29 ¶3 or "No possible abstract analog device can have more computation capabilities (up to polynomial time) than first-order recurrent networks" p154 in the box; ***Siegelmann*** *shows that it was well known to the person of ordinary skill in the art at the time the invention was made that the neural networks are universal computing machines, therefore it would have been obvious to the person of ordinary skill in the art at the time the invention was made to implement the output interpreter using a neural network, which the person of ordinary skill in the art at the time the invention was made would have logically understood to do using a second collection of hardware computing elements*).

Rationale:

de Garis and **Siegelmann** are from the same field of endeavor, neural networks. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of **de Garis** by using a neural network to implement the output interpreter would have been obvious because the use of neural networks as universal computing devices capable of performing any function as taught by **Siegelmann**, such as the translation performed by the output interpreter, because this was part of the ordinary capabilities of a person of ordinary skill in the art at the time the invention was made in view of the teachings above.

The combination of **de Garis** and **Siegelmann** fails to explicitly teach:

- the first collection of hardware elements and the second collection of hardware elements are different subsets of a third collection of hardware computing elements.

Azam teaches:

- the first collection of hardware elements and the second collection of hardware elements are different subsets of a third collection of hardware computing elements (p1-122 especially "construct an ensemble of neural networks arranged in some modular fashion" §2.3 or "integration of specialist modules" p22 ¶3 or "determination of the number and size of individual specialist modules within a modular neural network" §2.7.2 or Figure 5.2; *The person of ordinary skill in the art at the time the invention was made would have clearly understood how to apply this to modularly combining the networks detailed above*).

Rationale:

de Garis, **Siegelmann**, and **Azam** are from the same field of endeavor, neural networks. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the combined teachings of **de Garis** and **Siegelmann** by treating the two neural networks (Effector machines) as modules containing subsets of a larger neural network as taught by **Azam** for the benefit of finding optimal network topology and an appropriate set of neural network weights to accomplish the desired tasks (**Azam** p6 ¶3) in a manner that emulates the working principles of biological neural systems allowing the learning of new information while retaining old information and optimizing the information capacity of the neural pathways (**Azam** §1.4) since "modularity is key to the efficient and intelligent working of human and animal brains" (**Azam** p12 ¶1) or for greater flexibility in design and implementation (**Azam** §2.3) or scaling the structure of the network to match the complexity at least one task (**Azam** §5.4).

Claim Rejections - 35 USC § 103

Claims 13 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over **de Garis** ("The CAM-Brain Machine (CBM): an FPGA-based hardware tool that evolves a 1000 neuron-net circuit module in seconds and updates a 75 million neuron artificial brain for real-time robot control") as applied to claims 1-2, 5-6, 8, 10-12, 14-18, 21, 23-24, 26-28, 31-32, 34-35, 37-38, 43, 45, and 47-62 above, and further in view of **Mead** ("Analog VLSI and Neural Systems").

Claim 13:

de Garis fails to explicitly teach:

- wherein the hardware includes transistors configured to operate at or below a gate voltage at which the mobile charge in the transistor begins to limit the flow of current is called the threshold voltage.

Mead teaches:

- wherein the hardware includes transistors configured to operate at or below a gate voltage at which the mobile charge in the transistor begins to limit the flow of current is called the threshold voltage (pp36-39,67-81,208-209,260-263 especially p38-39).

Rationale:

Mead teaches that it is known to operate gate voltage subthreshold, or below the threshold at which the mobile charge begins to limit the flow of current. **Mead** discloses that there are many benefits for operating gates subthreshold, such as: power dissipation is extremely low, the drain current saturates allowing the transistor to operate as a current source for most of the voltage range, and the exponential nonlinearity is an ideal computation primitive for many applications (**Mead** p39). Thus the operation of a gate subthreshold was a particular known technique recognized as part of the ordinary capabilities of one skilled in the art. Therefore, the person of ordinary skill in the art at the time the invention was made would have found it obvious to apply this known technique to the hardware gates in the **de Garis** disclosure to achieve the benefits disclosed by **Mead**.

Claim 29:

de Garis teaches:

- limiting a range of values that at least one parameter of the Effectors is allowed to be set based on the error tolerance (p35-67 especially "preprogrammed to shut off the main clock when a temperature limit is exceeded" §5.3).

de Garis fails to explicitly teach:

- wherein said designing includes at least configuring transistors to operate at subthreshold, operating at subthreshold refers to operating below a gate voltage at which the mobile charge in the transistor begins to limit the flow of current is called the threshold voltage.

Mead teaches:

- wherein said designing includes at least configuring transistors to operate at subthreshold, operating at subthreshold refers to operating below a gate threshold voltage at which the mobile charge in the transistor begins to limit the flow of current (pp36-39,67-81,208-209,260-263 especially "gate voltage at which the mobile charge begins to limit the flow of current is called the threshold voltage" p38-39).

Rationale:

de Garis and **Mead** are from the same field of endeavor, analog neural systems. **Mead** teaches that it is known to operate gate voltage subthreshold, or below the threshold at which the mobile charge begins to limit

the flow of current. **Mead** discloses that there are many benefits for operating gates subthreshold, such as: power dissipation is extremely low, the drain current saturates allowing the transistor to operate as a current source for most of the voltage range, and the exponential nonlinearity is an ideal computation primitive for many applications (**Mead** p39). Thus the operation of a gate subthreshold was a particular known technique recognized as part of the ordinary capabilities of one skilled in the art. Therefore, the person of ordinary skill in the art at the time the invention was made would have found it obvious to apply this known technique to the hardware gates in the **de Garis** disclosure to achieve the benefits disclosed by **Mead**.

Claim Rejections - 35 USC § 103

Claims 36, 39, and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over **de Garis** ("The CAM-Brain Machine (CBM): an FPGA-based hardware tool that evolves a 1000 neuron-net circuit module in seconds and updates a 75 million neuron artificial brain for real-time robot control") as applied to claims 1-2, 5-6, 8, 10-12, 14-18, 21, 23-24, 26-28, 31-32, 34-35, 37-38, 43, 45, and 47-62 above, and further in view of **Azam** ("Biologically Inspired Modular Neural Networks").

Claim 36:

de Garis teaches:

- the collection of hardware computing elements is a first collection of hardware computing elements (p35-67 especially "neurons" §5.1),
- the Effector machine is a first Effector machine (p35-67 especially "artificial brain" §5.1), and

de Garis fails to explicitly teach:

- a subset of said Effectors are configured to receive information from a second Effector machine that is constructed form a second collection of hardware computing elements, and
- the first collection of hardware elements and the second collection of hardware elements are different subsets of a third collection of hardware computing elements.

Azam teaches:

- a subset of said Effectors are configured to receive information from a second Effector machine that is constructed form a second collection of hardware computing elements (1-122 especially "construct an ensemble of neural networks arranged in some modular fashion" §2.3 or Figure 5.2), and
- the first collection of hardware elements and the second collection of hardware elements are different subsets of a third collection of hardware computing elements (p1-122 especially "construct an ensemble of neural networks arranged in some modular fashion" §2.3 or "integration of specialist modules" p22 ¶3 or "determination of the number and size of individual specialist modules within a modular neural network" §2.7.2 or Figure 5.2; *The person of ordinary skill in the art at the time the invention was made would have clearly understood how to apply this to modularly combining the networks detailed above*).

Rationale:

de Garis and **Azam** are from the same field of endeavor, neural networks. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of **de Garis** by treating the two neural networks (Effector machines) as modules where one module receives information from another module, each module containing subsets of a larger neural network as taught by **Azam** for the benefit of finding optimal network topology and an appropriate set of neural network weights to accomplish the desired tasks (**Azam** p6 ¶3) in a manner that emulates the working principles of biological neural systems allowing the learning of new information while retaining old information and optimizing the information capacity of the neural pathways (**Azam** §1.4) since "modularity is key to the efficient and intelligent working of human and animal brains" (**Azam** p12 ¶1) or for greater flexibility in design and implementation (**Azam** §2.3) or scaling the structure of the network to match the complexity at least one task (**Azam** §5.4).

Claim 39:

de Garis fails to explicitly teach:

- at least changing a number of representations of modules in a representation of the machine.

Azam teaches:

- at least changing a number of representations of modules in a representation of the machine (p1-122 especially "construct an ensemble of neural networks arranged in some modular fashion" §2.3 or "integration

of specialist modules" p22 ¶3 or "determination of the number and size of individual specialist modules within a modular neural network" §2.7.2 or Figure 5.2).

Rationale:

de Garis and **Azam** are from the same field of endeavor, neural networks. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of **de Garis** by modifying the number of as taught by **Azam** for the benefit of finding optimal network topology and an appropriate set of neural network weights to accomplish the desired tasks (**Azam** p6 ¶3) in a manner that emulates the working principles of biological neural systems allowing the learning of new information while retaining old information and optimizing the information capacity of the neural pathways (**Azam** §1.4) since "modularity is key to the efficient and intelligent working of human and animal brains" (**Azam** p12 ¶1) or for greater flexibility in design and implementation (**Azam** §2.3) or scaling the structure of the network to match the complexity at least one task (**Azam** §5.4).

Claim 40:

de Garis fails to explicitly teach:

- at least changing a number of software Effectors per software module.

Azam teaches:

- wherein said evolving of the graph includes at least changing a number of software Effectors per software module (p1-122 especially "nodes are trying to evolve" §3.2 or "evaluated to detect obsolete and ineffective weight connections or neurons in the neural network model which then are removed before further evolution of architecture" §5.2 or "Dynamic node creation" §5.3).

Rationale:

de Garis and **Azam** are from the same field of endeavor, neural networks. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of **de Garis** by modifying the number of as taught by **Azam** for the benefit of finding optimal network topology and an appropriate set of neural network weights to accomplish the desired tasks (**Azam** p6 ¶3) in a manner that emulates the working principles of biological neural systems allowing the learning of new information while retaining old information and optimizing the information capacity of the neural pathways (**Azam** §1.4) or for greater flexibility in design and implementation (**Azam** §2.3) or scaling the structure of the network to match the complexity at least one task (**Azam** §5.4).

Claim Rejections - 35 USC § 103

Claims 41-42 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over **de Garis** ("The CAM-Brain Machine (CBM): an FPGA-based hardware tool that evolves a 1000 neuron-net circuit module in seconds and updates a 75 million neuron artificial brain for real-time robot control") as applied to claims 1-2, 5-6, 8, 10-12, 14-18, 21, 23-24, 26-28, 31-32, 34-35, 37-38, 43, 45, and 47-62 above, and further in view of **Marian** ("A biologically inspired model of motor control of direction").

Claim 41:

de Garis fails to explicitly teach:

- at least changing one or more refractory periods associated with one or more software Effectors.

Marian teaches:

- at least changing one or more refractory periods associated with one or more software Effectors (p1-181 especially §4.3.1 or §4.3.3 or Algorithm 1 or Algorithm 3 or Table 5.3).

Rationale:

de Garis and **Marian** are from the same field of endeavor, pulsed/spiked neural networks. **Marian** describes the effect of modifying various variables in such a network, such as refractory periods. Thus, all claimed elements were known in the prior art and the person of ordinary skill in the art at the time the invention was made could have combined the elements as claimed, by modifying the teachings of **de Garis** by changing one or more refractory periods, as taught by **Marian**, with no change in the respective functions of the elements, and the combination would have yielded predictable results to one of ordinary skill in the art at the time of the invention.

Claim 42:

de Garis fails to explicitly teach:

- at least changing one or more thresholds associated with one or more software Effectors associated with the graph.

Marian teaches:

- at least changing one or more thresholds associated with one or more software Effectors associated with the graph (p1-181 especially §4.3.1 or §5.1 or §5.3.2 or Table 5.3).

Rationale:

de Garis and **Marian** are from the same field of endeavor, pulsed/spiked neural networks. **Marian** describes the effect of modifying various variables in such a network, such as thresholds. Thus, all claimed elements were known in the prior art and the person of ordinary skill in the art at the time the invention was made could have combined the elements as claimed, by modifying the teachings of **de Garis** by changing one or more thresholds, as taught by **Marian**, with no change in the respective functions of the elements, and the combination would have yielded predictable results to one of ordinary skill in the art at the time of the invention.

Claim 44:

de Garis fails to explicitly teach:

- at least changing one or more representation of amplitudes associated with one or more representations of Effectors associated with the graph.

Marian teaches:

- at least changing one or more representation of amplitudes associated with one or more representations of Effectors associated with the graph (p1-181 especially §2.1.2 or §7.2.1).

Rationale:

de Garis and **Marian** are from the same field of endeavor, pulsed/spiked neural networks. **Marian** describes the effect of modifying various variables in such a network, such as amplitudes. Thus, all claimed elements were known in the prior art and the person of ordinary skill in the art at the time the invention was made could have combined the elements as claimed, by modifying the teachings of **de Garis** by changing one or more amplitudes, as taught by **Marian**, with no change in the respective functions of the elements, and the combination would have yielded predictable results to one of ordinary skill in the art at the time of the invention.

Claim Rejections - 35 USC § 103

Claim 46 is rejected under 35 U.S.C. 103(a) as being unpatentable over **de Garis** ("The CAM-Brain Machine (CBM): an FPGA-based hardware tool that evolves a 1000 neuron-net circuit module in seconds and updates a 75 million neuron artificial brain for real-time robot control") as applied to claims 1-2, 5-6, 8, 10-12, 14-18, 21, 23-24, 26-28, 31-32, 34-35, 37-38, 43, 45, and 47-62 above, and further in view of **Atsumi** ("Artificial Neural Development for Pulsed Neural Network Design – A Simulation Experiment on Animat's Cognitive Map Genesis").

Claim 46:

de Garis fails to explicitly teach:

- at least changing one or more representations of conduction time associated with representations of the Effectors.

Atsumi teaches:

- at least changing one or more representations of conduction time associated with representations of the Effectors (p188-197 especially p191 C2 ¶1-2).

Rationale:

de Garis and **Marian** are from the same field of endeavor, pulsed/spiked neural networks. **Atsumi** describes the effect of modifying various variables in such a network, such as conduction times. Thus, all claimed elements were known in the prior art and the person of ordinary skill in the art at the time the invention was made could have combined the elements as claimed, by modifying the teachings of **de Garis** by changing one or more conduction times, as taught by **Atsumi**, with no change in the respective functions of the elements, and the combination would have yielded predictable results to one of ordinary skill in the art at the time of the invention.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Hérault ("Optimization by pulsed recursive neural networks")
- Gallagher ("Continuous Time Recurrent Neural Networks: A Paradigm for Evolvable Analog Controller Circuits")
- Floreano ("Evolution of Spiking Neural Controllers for Autonomous Vision-Based Robots")

Claims 1, 2, 5, 6, 8-18, 21, 23-29, 31, 32, and 34-62 are rejected.

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Benjamin Buss whose telephone number is 571-272-5831. The examiner can normally be reached on M-F 9AM-5PM.

As detailed in MPEP 502.03, communications via Internet e-mail are at the discretion of the applicant. Without a written authorization by applicant in place, the USPTO will not respond via Internet e-mail to any Internet correspondence which contains information subject to the confidentiality requirement as set forth in 35 U.S.C. 122. A paper copy of such correspondence will be placed in the appropriate patent application. The following is a sample authorization form which may be used by applicant:

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Vincent can be reached on 571-272-3080. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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